WHAT IS CLAIMED IS:

1. An apparatus for mapping and spreading data symbols in a mobile communication system when quadrature phase shift keying modulation is performed in a mobile communication time division duplex mode, the apparatus mapping and spreading the data symbols by using binary operations.

2. The apparatus of claim 1, which maps and spreads the data symbols by using the binary operations, instead of using complex number operations, to improve efficiency of the mobile communication system.

3. The apparatus of claim 1, comprising:

a binary channelized data symbol generator for generating imaginary coefficients of binary information mapped symbols;

a binary counter for counting the imaginary coefficients;

a first XOR circuit for calculating XOR values for the most significant bit and the least significant bit of the binary counter, and outputting the resulting values;

a binary scrambling code generator for mapping a scrambling code to 0 and 1, and outputting the mapped values;

a second XOR circuit for calculating XOR values for the output value from the binary scrambling code generator, the output value from the first XOR circuit, and a real coefficient of the symbol mapped by the binary channelized data symbol generator;

a mapper for mapping the values calculated by the second XOR circuit to binary numbers, and outputting the mapped values; and

a switch for outputting the output values from the mapper to a real part and an imaginary part according to the least significant bit of the binary counter,

wherein the values calculated by the second XOR circuit are binary numbers such as 0 and 1 divided into a real part and an imaginary part.

4. An apparatus for mapping and spreading data symbols in a mobile communication system, comprising:

a binary counter for counting imaginary coefficients of symbols mapped by a binary channelized data symbol generator;

a first XOR circuit for calculating XOR values for the most significant bit and the least significant bit of the binary counter, and outputting the resulting values;

a binary scrambling code generator for mapping a scrambling code to 0 and 1, and outputting the mapped values;

a second XOR circuit for calculating XOR values for the output value from the binary scrambling code generator, the output value from the first XOR circuit, and a real coefficient of the symbol mapped by the binary channelized data symbol generator;

a mapper for mapping the values calculated by the second XOR circuit to binary numbers, and outputting the mapped values; and

a switch for outputting the output values from the mapper to a real part and an imaginary part according to the least significant bit of the binary counter,

wherein the values calculated by the second XOR circuit are binary numbers divided into a real part and an imaginary part.

5. The apparatus of claim 4, wherein the mapper maps the binary number 0 to the binary number 1, and maps the binary number 1 to the binary number –1.

6. The apparatus of claim 4, wherein the binary channelized data symbol generator comprises:

a weight sign binary unit for outputting binary numbers corresponding to a sign of a weight, and outputting the binary numbers corresponding to an imaginary number of the weight;

a binary symbol unit for XORing two consecutive bit sequences, dividing the resulting values into real and imaginary parts through an inverter circuit, switching the real and imaginary parts according to the binary numbers from the weight sign binary unit corresponding to the imaginary number, and outputting the switched parts;

a binary orthogonal variable spreading factor code generator for mapping an orthogonal variable spreading factor code generated by selection of a spreading factor to 0 and 1, and outputting the mapped values;

a binary channelizer for XORing the binary number from the binary symbol unit divided into the real and imaginary parts, the binary number from the weight sign binary unit and the binary number from the binary orthogonal variable spreading factor code generator, and outputting the resulting values; and

a second switch for selectively outputting the XORed values from the binary channelizer.

7. The apparatus of claim 6, wherein the second switch selectively outputs 0 and 1 from the binary channelizer divided into the real and imaginary parts.

8. The apparatus of claim 6, wherein the binary symbol unit comprises:

a third XOR circuit for XORing the two consecutive bit sequences, and outputting the resulting values;

an inverter circuit for generating an imaginary part by inverting a bit from the third XOR circuit, and outputting the imaginary part; and

a third switch for selectively switching an output bit from the third XOR circuit corresponding to the real part and an output bit from the inverter circuit corresponding to the imaginary part according to a bit for notifying the imaginary part of the weight in the weight sign binary unit.

9. The apparatus of claim 6, wherein the binary channelizer comprises:

a fourth XOR circuit for XORing a bit for deciding the sign of the symbol corresponding to the consecutive bit sequences in the binary symbol unit, a bit for notifying the sign of the weight in the weight sign binary unit, and a bit sequence based on the binary orthogonal variable spreading factor code in the binary orthogonal variable spreading factor code generator, and outputting the resulting values;

a fifth XOR circuit for XORing a bit for notifying the imaginary number of the weight in the weight sign binary unit and a bit sequence from the fourth XOR circuit, and outputting the resulting values; and

a flip-flop for storing a bit corresponding to the imaginary part from the binary symbol unit until the orthogonal variable spreading factor code is generated.

10. A method of mapping and spreading data symbols in a mobile communication system, comprising:

generating imaginary coefficients of binary information mapped symbols;

counting said imaginary coefficients;

calculating first exclusive-OR values for a most significant bit and a least significant bit of the count value;

outputting said calculated first exclusive-OR values;

mapping a scrambling code to binary numbers;

outputting mapped values;

calculating second exclusive-OR values for said outputted mapped values, said outputted calculated first exclusive-OR values, and a real coefficient of one of said mapped symbols;

mapping said calculated second exclusive-OR values to binary numbers;

outputting said mapped calculated second exclusive-OR values; and

outputting said outputted mapped calculated second exclusive-OR values to a real part and an imaginary part according to said least significant bit.

11. The method of claim 10, wherein said calculated second exclusive-OR values are binary numbers which are divided into a real part and an imaginary part.

12. The method of claim 10, wherein quadrature phase shift keying modulation is performed in the mobile communication system in a mobile communication time division duplex mode.

13. A method of mapping and spreading data symbols in a mobile communication system, comprising:

performing data symbol mapping; and

performing data symbol spreading,

wherein said data symbols are mapped and spread using binary operations.

14. The method of claim 13, further comprising:

generating imaginary coefficients of binary information mapped symbols;

counting said imaginary coefficients;

calculating first exclusive-OR values for a most significant bit and a least significant bit of the count value;

outputting said calculated first exclusive-OR values;

mapping a scrambling code to binary numbers;

outputting mapped values;

calculating second exclusive-OR values for said outputted mapped values, said outputted calculated first exclusive-OR values, and a real coefficient of one of said mapped symbols;

mapping said calculated second exclusive-OR values to binary numbers;

outputting said mapped calculated second exclusive-OR values; and

outputting said outputted mapped calculated second exclusive-OR values to a real part and an imaginary part according to said least significant bit.